

74F656A

Octal buffer/driver with parity; non-inverting; 3-state

Rev. 6 — 14 December 2011

Product data sheet

1. General description

The 74F656A is an octal buffer and line driver with parity generation/checking. The 74F656A can be used as memory address driver, clock driver and bus-oriented transmitter/receiver. The inclusion of parity generation/checking improves PCB density.

2. Features and benefits

- Combines 74F244 and 74F280A functions in one device
- High impedance NPN base inputs for reduced input current (40 μ A in HIGH and LOW states)
- I_{IL} = 20 μ A compared to 600 μ A in FAST family specification
- For applications with high output drive and light bus loading
- Non-inverting
- 3-state output sink capability I_{OL} = 64 mA and source I_{OH} = 15 mA
- Inputs and outputs on separate sides simplifies board layout
- Combined functions reduce part count and enhance system performance
- Industrial temperature range available (–40 °C to +85 °C)

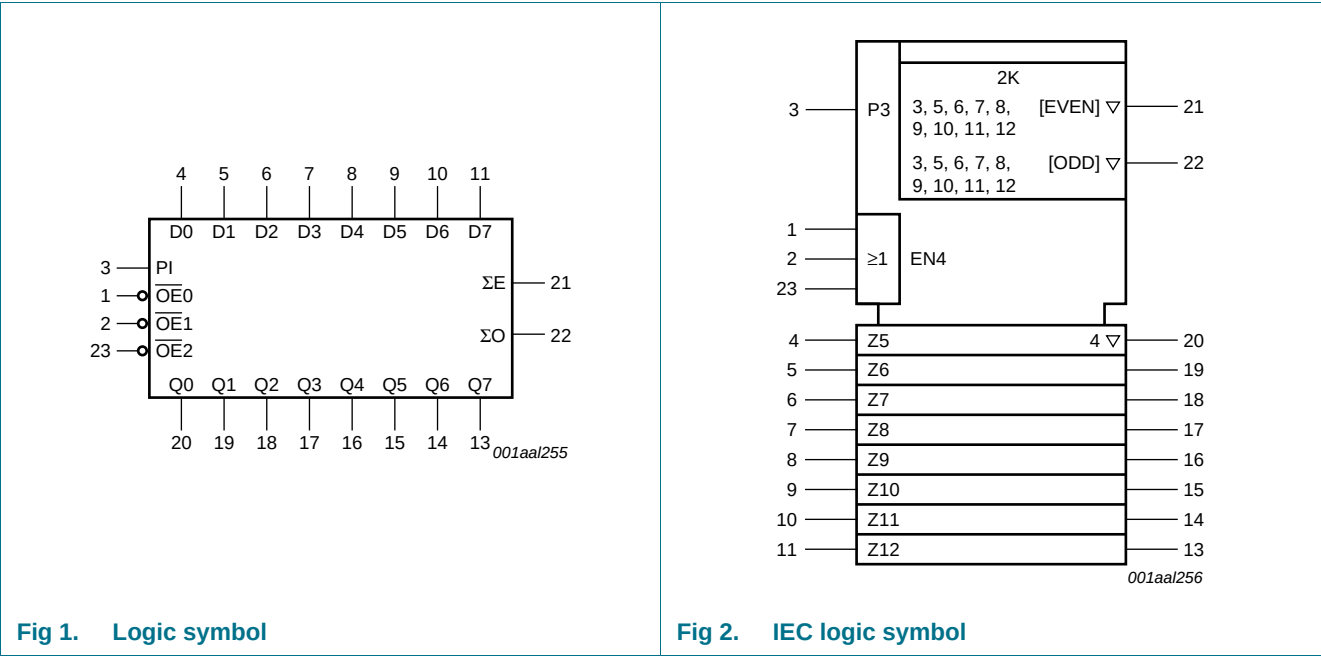
3. Ordering information

Table 1. Ordering information

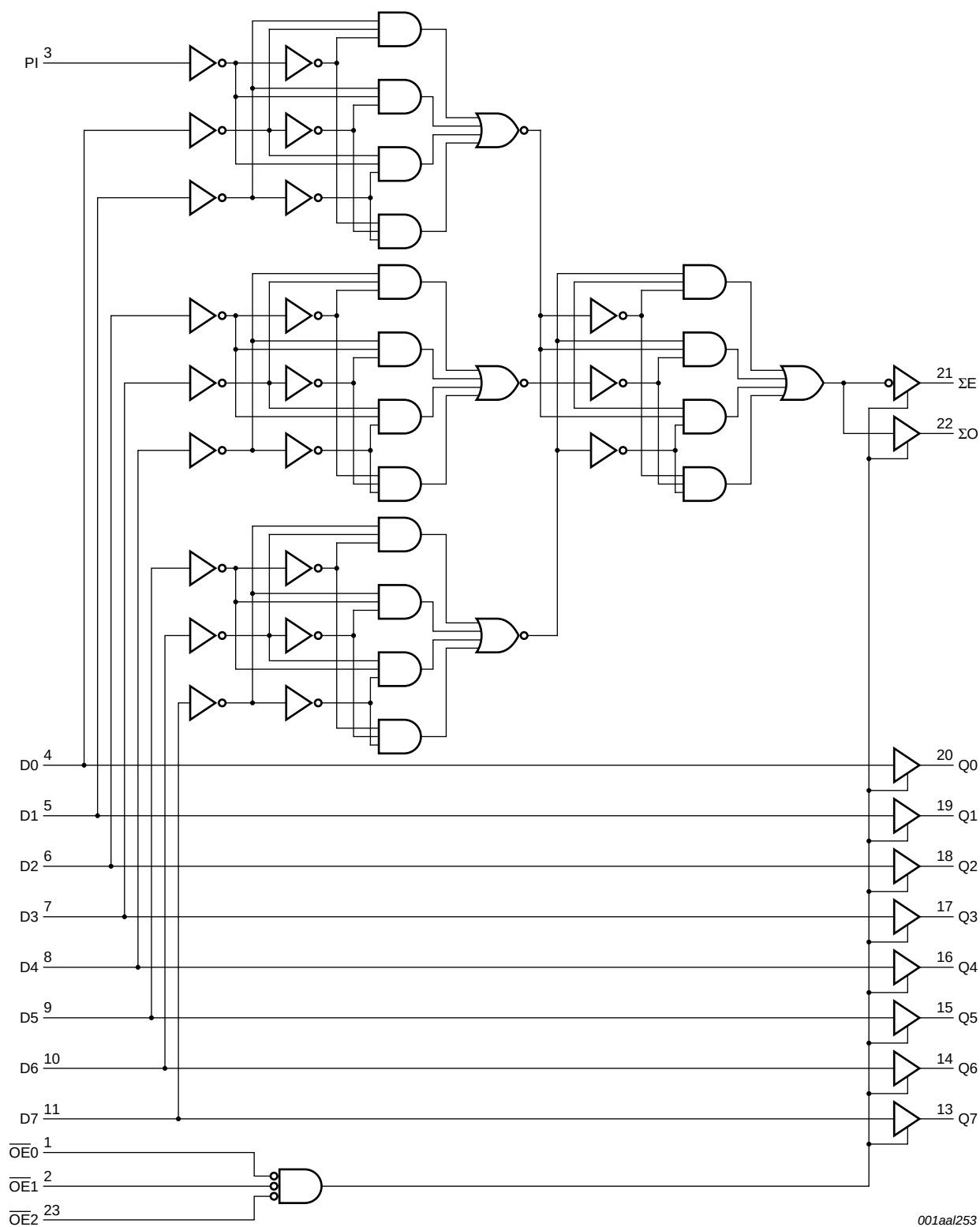
Type number	Package			
	Temperature range	Name	Description	Version
N74F656AD	0 °C to 70 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
I74F656AD	–40 °C to +85 °C			



4. Functional diagram



The IEC logic symbol for the 74F656A is a rectangular block. On the left edge, inputs are labeled: P3 (pin 3), EN4 (pins 1 and 2, with a '≥1' symbol), and a series of inputs Z5 through Z12 (pins 4, 5, 6, 7, 8, 9, 10, 11). On the right edge, outputs are labeled: 2K [EVEN] (pin 21), 2K [ODD] (pin 22), 4 (pin 20), and a series of outputs Z6 through Z12 (pins 19, 18, 17, 16, 15, 14, 13). The identifier '001aal256' is located at the bottom right of the symbol.



001aa1253

Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

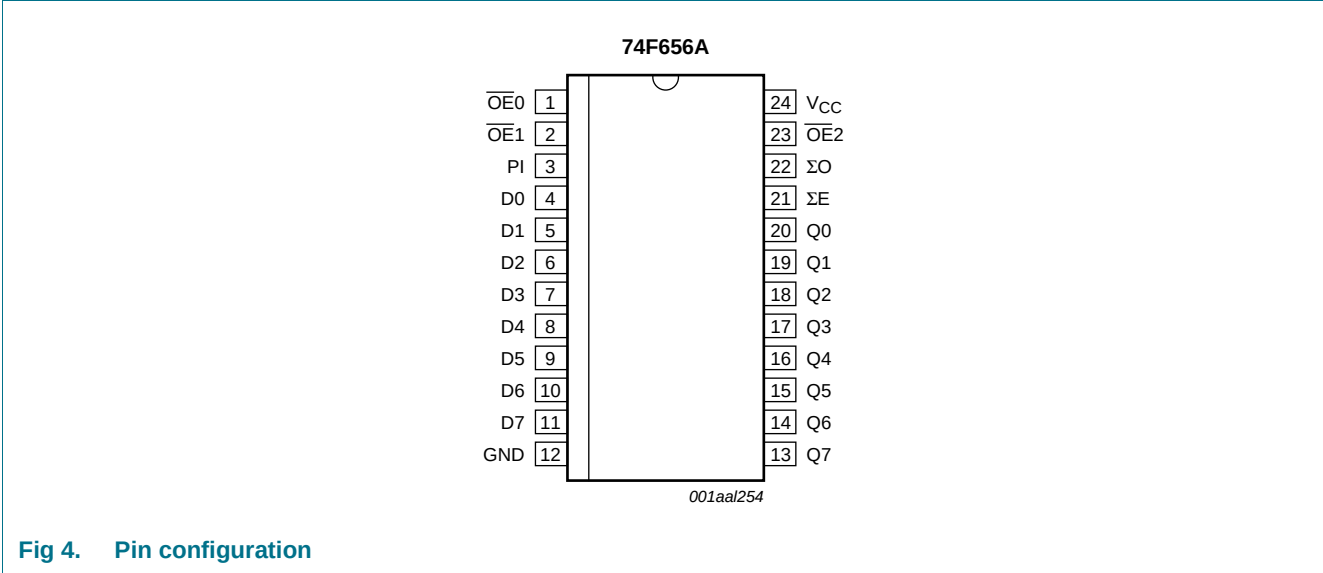


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description	Unit load HIGH/LOW	Load value ^[1] HIGH/LOW
$\overline{\text{OE0}}$	1	output enable input (active LOW)	1.0/0.033	20 μA /20 μA
$\overline{\text{OE1}}$	2	output enable input (active LOW)	1.0/0.033	20 μA /20 μA
PI	3	parity input	1.0/0.033	20 μA /20 μA
D0 to D7	4, 5, 6, 7, 8, 9, 10, 11	data input	2.0/0.066	40 μA /40 μA
GND	12	ground (0 V)		
Q0 to Q7	20, 19, 18, 17, 16, 15, 14, 13	data output	750/106.7	15 mA/64 mA
ΣE	21	even parity output	750/106.7	15 mA/64 mA
ΣO	22	odd parity output	750/106.7	15 mA/64 mA
$\overline{\text{OE2}}$	23	output enable input (active LOW)	1.0/0.033	20 μA /20 μA
V _{CC}	24	supply voltage		

[1] One FAST Unit Load (UL) is defined as 20 μA in HIGH state, 0.6 μA in LOW state.

6. Functional description

6.1 Function table

Table 3. Function selection^[1]

Input				Output	Status
OE0	OE1	OE2	Dn	Qn	
L	L	L	L	L	transparent
L	L	L	H	H	
H	X	X	X	Z	disabled
X	H	X	X	Z	
X	X	H	X	Z	

[1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

Table 4. Function parity outputs^[1]

Inputs	State	Parity output	
		ΣE	ΣO
Even number of inputs (0, 2, 4, 6, 8)	H	H	L
Odd number of inputs (1, 3, 5, 7, 9)	H	L	H
Any $\overline{OEn}$	H	Z	Z

[1] H = HIGH voltage level;
 L = LOW voltage level;
 Z = high-impedance OFF-state.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		^[1] -0.5	+7.0	V
V_O	output voltage	output in HIGH-state	^[1] -0.5	V_{CC}	V
I_{IK}	input clamping current	$V_I < 0$ V	-30	+5	mA
I_O	output current	output in LOW-state	-	128	mA
T_{amb}	ambient temperature	in free-air	^[2]		
		commercial	0	70	°C
		industrial	-40	+85	°C
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{IK}	input clamping current		-	-	-18	mA
I_{OH}	HIGH-level output current		-15	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA

9. Static characteristics

Table 7. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5$ V; $I_{IK} = -18$ mA	-1.2	-0.73	-	-1.2	-	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 4.5$ V; $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V						
		$I_{OH} = -3$ mA						
		$V_{CC} = \pm 10$ %	-	-	-	2.4	-	V
		$V_{CC} = \pm 5$ %	-	3.3	-	2.7	-	V
		$I_{OH} = -15$ mA						
		$V_{CC} = \pm 10$ %	-	-	-	2.0	-	V

Table 7. Static characteristics ...continued

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; V _{IL} = 0.8 V; V _{IH} = 2.0 V						
		I _{OL} = 64 mA						
		V _{CC} = ±10 %	-	-	-	-	0.55	V
		V _{CC} = ±5 %	-	0.42	-	-	0.55	V
I _I	input leakage current	V _{CC} = 0 V; V _I = 7.0 V	-	-	-	-	100	μA
I _{IH}	HIGH-level input current	V _{CC} = 5.5 V; V _I = 2.7 V; commercial						
		pin Dn	-	-	-	-	40	μA
		pin PI, $\overline{\text{OEn}}$	-	-	-	-	20	μA
		V _{CC} = 5.5 V; V _I = 2.7 V; industrial						
		pin Dn	-	-	-	-	80	μA
		pin PI, $\overline{\text{OEn}}$	-	-	-	-	40	μA
I _{IL}	LOW-level input current	V _{CC} = 5.5 V; V _I = 0.5 V						
		pin Dn	-	-	-	-	–40	μA
		pin PI, $\overline{\text{OEn}}$	-	-	-	-	–20	μA
I _{OZ}	OFF-state output current	V _{CC} = 5.5 V						
		V _O = 2.7 V	-	-	-	-	50	μA
		V _O = 0.5 V	-	-	-	-	–50	μA
I _O	output current	V _{CC} = 5.5 V ^[2]	-	-	-	–100	–225	mA
I _{CC}	supply current	V _{CC} = 5.5 V; V _I = GND or V _{CC}						
		outputs HIGH-state	-	50	-	-	80	mA
		outputs LOW-state	-	78	-	-	110	mA
		outputs OFF-state	-	83	-	-	90	mA

[1] All typical values are measured at V_{CC} = 5 V.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

10. Dynamic characteristics

Table 8. Dynamic characteristics

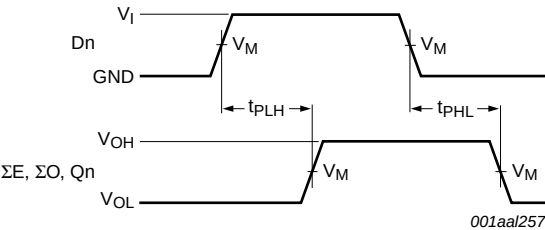
GND = 0 V; for test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			0 °C to 70 °C; V _{CC} = 5.0 V ± 0.5 V		–40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	Dn to Qn; see Figure 5	2.0	4.0	6.5	2.0	7.0	2.0	8.0	ns
		Dn to ΣE, ΣO; see Figure 5	5.5	10.0	13.0	5.5	14.0	4.5	16.5	ns
t _{PHL}	HIGH to LOW propagation delay	Dn to Qn; see Figure 5	2.5	5.5	7.0	2.5	7.5	2.5	9.0	ns
		Dn to ΣE, ΣO; see Figure 5	5.5	11.0	14.5	5.5	16.5	5.5	18.0	ns
t _{PZH}	OFF-state to HIGH propagation delay	$\overline{\text{OEn}}$ to Qn; see Figure 6	3.5	7.0	10.5	3.5	11.5	3.0	13.0	ns

Table 8. Dynamic characteristics ...continued
GND = 0 V; for test circuit, see Figure 7.

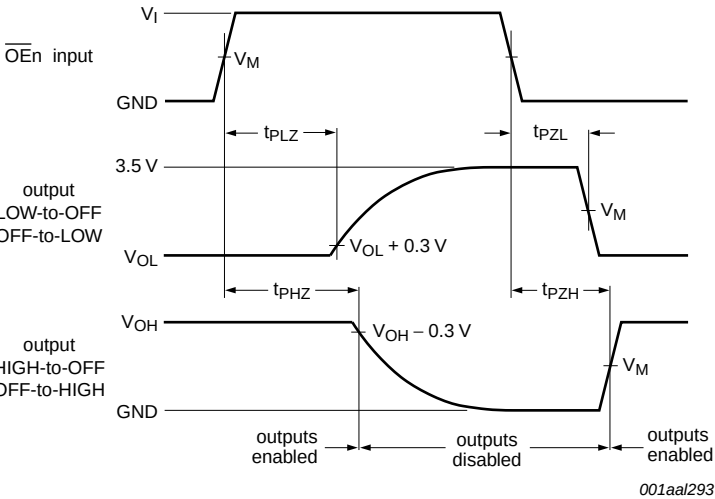
Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			0 °C to 70 °C; V _{CC} = 5.0 V ± 0.5 V		−40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PZL}	OFF-state to LOW propagation delay	$\overline{\text{OEn}}$ to Qn; see Figure 6	4.0	8.0	11.0	4.5	12.0	4.0	13.5	ns
t _{PHZ}	HIGH to OFF-state propagation delay	$\overline{\text{OEn}}$ to Qn; see Figure 6	1.5	4.5	8.0	1.5	9.0	1.5	10.0	ns
t _{PLZ}	LOW to OFF-state propagation delay	$\overline{\text{OEn}}$ to Qn; see Figure 6	2.0	5.0	8.0	2.0	9.0	1.5	10.0	ns

11. Waveforms



V_M = 1.5 V

Fig 5. Propagation delay input Dn to output Qn, ΣE, ΣO



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. 3-state output enable and disable times

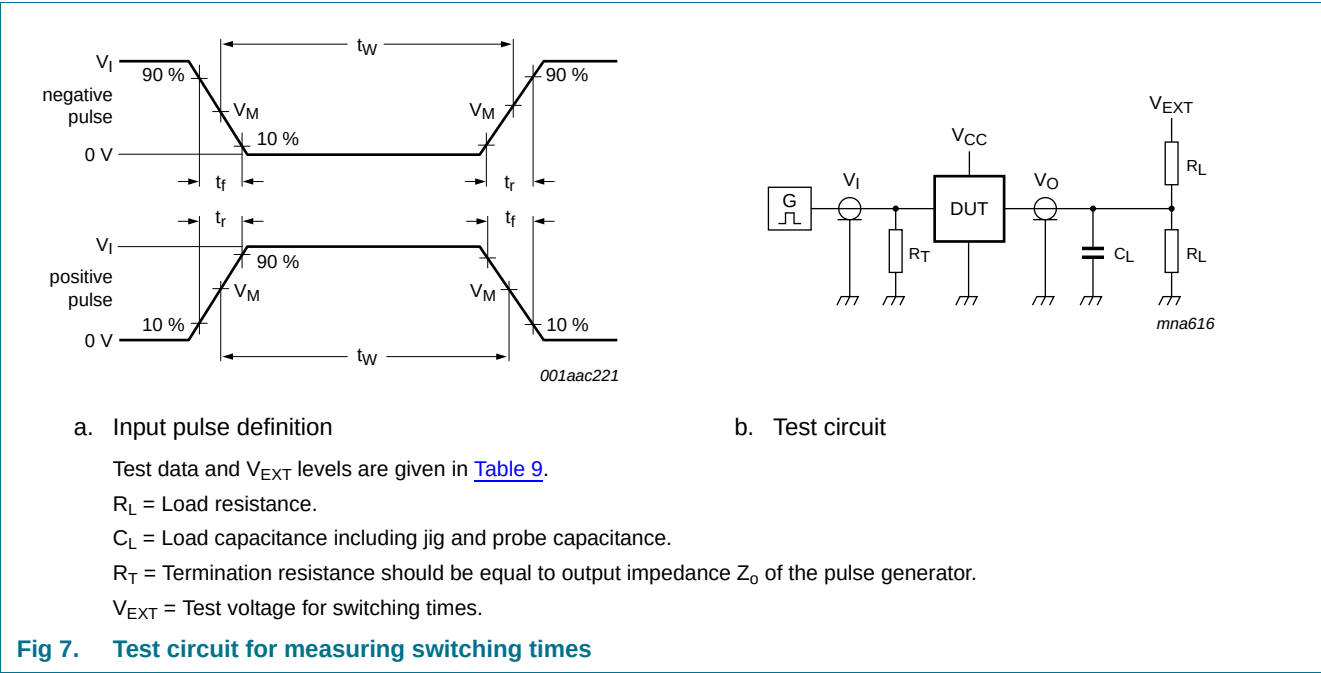


Fig 7. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

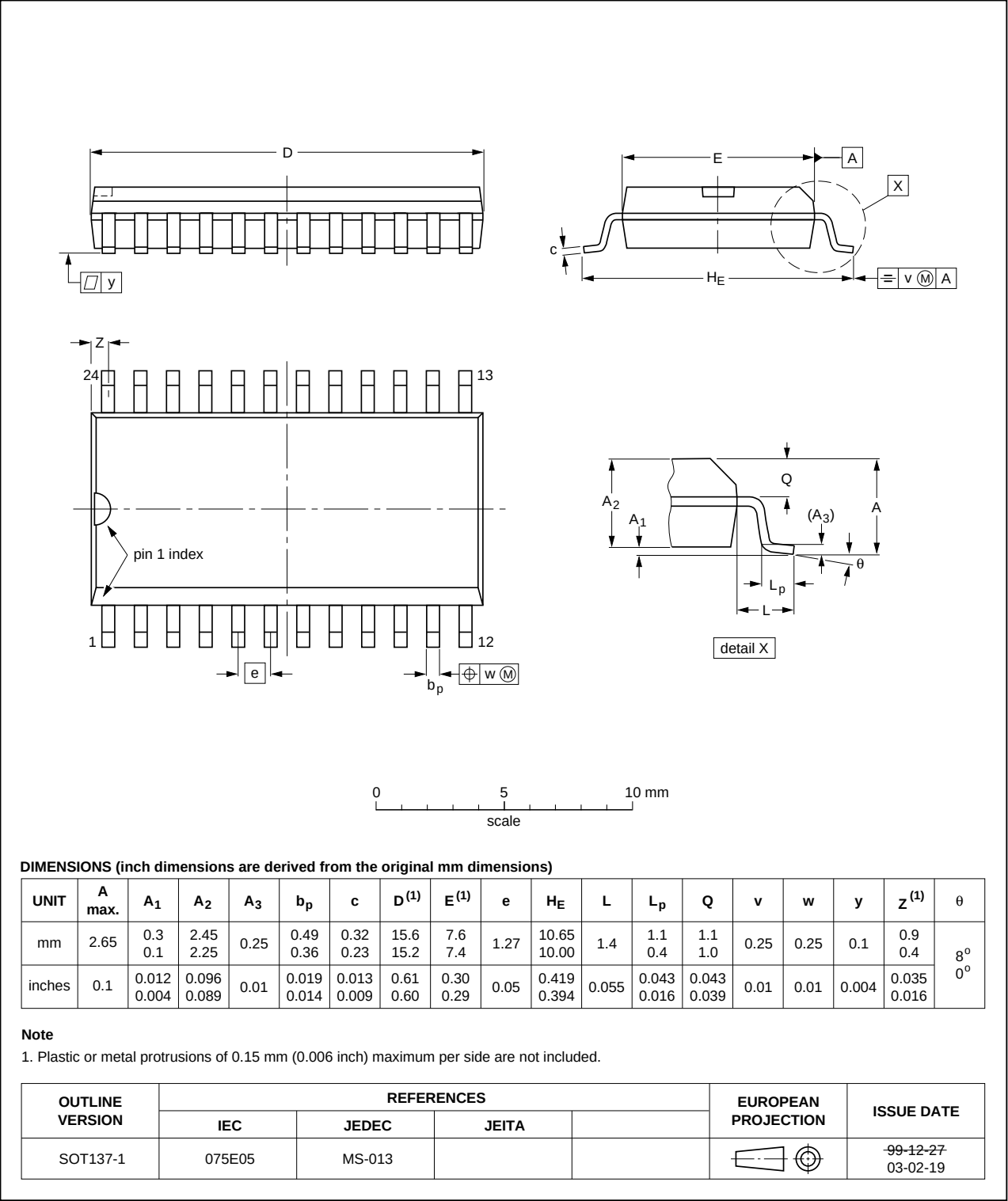


Fig 8. Package outline SOT137-1 (SO24)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PCB	Printed-Circuit Board

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74F656A v.6	20111214	Product data sheet	-	74F656A v.5
Modifications:	• Legal pages updated.			
74F656A v.5	20100325	Product data sheet	-	74F656A v.4
74F656A v.4	20100205	Product data sheet	-	74F656A v.3
74F656A v.3	20000630	Product specification	-	74F656A v.2
74F656A v.2	19910717	Product specification	-	-

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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